Leadframe Package Design Collaboration

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History of lead frame packaging

- DIP (Dual In-line Package) (1972) Up to 48 pins
- SOP (Small Outline Package) (1980) Up to 48 surface mount pins
- QFP (Quad Flat Package) (1985) Up to 304 surface mount pins
- QFN (Quad Flat No-leads) (1986) Up to 80 surface mount pins
- Fusion Quad (2009) Up to 400 surface mount pins (QFN and QFP combined)
Factors affecting package design

- Area – driven to reduce
- Thickness – driven to reduce
- Pin count – driven to increase
- Cost – driven to reduce
- Electrical characteristics – Higher frequencies demand better performance
- Thermal conductivity – Hotter dies demand better heat dissipation
- Reliability – always a driver
Reasons why Lead Frames are now in greater demand

- Ability to handle pin counts up to 400. These are useful for many small form factor applications and make for an attractive solution with SOC applications.
- Much lower cost as compared to organic substrates.
- Ability to do accurate SI/PI analysis of single and stacked packages has removed an earlier impediment to this choice.
Drivers for move towards die co-design and analysis of lead frame packages

- Increasing usage of lead frames for high pin count dies
- Usage of lead frames for stacked die package configurations
- Higher frequencies requiring bond wires and gull wing effects to be included in the electrical analysis
- Greater thermal load from higher power devices creates the need for thermal analysis
- Ability to use off the shelf lead frames rather than custom substrates reduces time to market
- Complex Packages need SI / PI analysis
Cadence and CAD Design Software
Why work together?

- CAD Design Software is a long term supplier of leadframe design solutions
- Cadence is the market leading design solution for multi-layer wirebond and flip-chip packages
- Joint decision to partner instead of build two separate solutions
- Many customers looking for a joint solution due to the need to address:
  - Die stacking, complex wirebonding, EM and thermal modeling
What we do today

• Leadframe Design Flow
  – CDS has the links to AutoCAD – Cadence can wirebond and co-design

  – Usage of actual bondwire profiles and bonding diagram output are an integral part of this joint flow making for a more reliable and coherent flow

  – Reliability is vastly improved using a flow that augments design capabilities in AutoCAD and provides a complete and robust link to analysis of the complete package in APD/SiP
Joint Solution Flow

CDS Extensions to AutoCAD create accurate leadframe paddle

Create gull wing to lead tip netlist with power rings

Intelligize AutoCAD data in preparation for APD / SiP export

Import intelligent leadframe library object (paddle) and establish netlist from die information

Assign wirebond profiles for die to lead connections and make connections

Leadframe design now available for 3D DRC, extraction for 3D modeling tools, etc.
Clean AutoCad Data (closed polygons, removed duplicate lines) intelligized to understand lead tips / ends
Add intelligence to Leadframe mechanical data
Example: Gull wing definition
Create SKILL data for APD / SiP
Import data into APD / SiP
Imported leadframe in APD / SiP
Importing Die into APD / SiP showing connectivity
Wirebonding the die to leads and pwr / gnd bars
Visualize and check the design in 3D
Additional Information

- Available to designer
  - Die stacking with complex wirebonding
  - 3D DRC (wire to wire spacing)
  - Package modeling
  - Chip-package optimization
  - Chip-Package-Board SI and PI analysis
  - Manufacturing artwork
    » Wire diagrams
What we plan for the future

• Roadmap
  – Chip-Package Co-Design
    • Cadence is evolving co-design technology beyond tightly integrated solutions with IC Design tools to easier more flexible models - i.e. distributed co-design
  – Extraction
    • 3D extraction partners work as an engine under the Cadence SiP signal and power integrity environment
      – Apache PakSi-E (today)
      – CST Microwave Studio (2H 2010)
      – Others
  – Cost optimization of design (reduce gold cost)
  – PCB in leadframe (is this a requirement for you?)
Summary

- Historically EDA design support for leadframes has been limited
- Complexity of today’s leadframes requires sophisticated wirebond and package extraction technology
- Cadence and CDS have teamed up to provide a smooth path from mechanical (AutoCAD) design of the leadframe paddle to an intelligent APD / SiP design that can be wirebonded, 3D DRC’d, and analyzed using signal and power integrity solutions.
  - Integration with Chip and PCB design allows for an optimized system design.
- For more information:
  - Visit TeamAllegro on Cadence Blogs, LinkedIn, Facebook, Twitter
EPD
Create/ edit existing QFP / QFN Lead Frame Drawings

CDS EPD Intelligizing

LIBRARY
AutoCAD Lead frame

EPD 2 SKL Converter

LIBRARY
APD Symbols & Design Rules

• Online 2D spacing DRC
• Electrical constraints
• Batch assembly rule checks
• Batch 3D interference checks
• Final connectivity check

APD / SiP
Create/ import netlist

Create/ import Bondwire profile

Wire bonding

Completed Design

Create Stack

Create/ import dies

Data export
• Wire bond pattern (XML)
• DXF for OLP
• Artwork (Gerber, AIF, DXF)

REPORTS
• DRC report
• Wire bond placement report
• 3D wire usage report

Extracta
2 and 2.5 D data for thermal, mechanical and other simulation and analysis
Simpler view of previous slide

- **CAD Design Software - EPD**
  - Autocad extensions focused on lead paddle design
  - Intelligize AutoCad data in preparation for APD / SiP export
    - Create gull wing to lead tip netlist with power rings
    - Library of leadframes available for Cadence

- **Cadence SiP / APD**
  - Import intelligent leadframe library object (paddle)
  - Establish netlist from die information
  - Assign wirebond profiles for die to lead connections
  - Leadframe exists as a normal package design in APD / SiP
    - Die stacking with complex wirebonding, DRC, package modeling, chip-package optimization, manufacturing artwork all available to designer